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REMARKS

Claims 1, 3-9, 11-17 and 19-28 stand finally rejected. More particularly, claims 1, 3-6, 9, 11-15, 19-23, 26 and 28 stand rejected under 35 U.S.C. 102(c) as being anticipated by U.S. Patent No. 6,559,538 to Pomerene et al. In addition, claims 7, 8, 16-18, 24, 25, 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Pomerene et al. in view of U.S. Patent No. 6,476,483 to Adler et al. Applicants respectfully request reconsideration of the Examiner's rejection of claims 1, 3-9, 11-17 and 19-28.

Rejections under 35 U.S.C. 102(e)

The Examiner's position regarding the alleged teachings of Pomerene et al. are set forth on page 2 of the instant Office Action. The Examiner has taken the position that Pomerene et al. discloses a Peltier effect heat transfer device positioned in an insulating substrate. The structure identified by the Examiner as constituting an insulating substrate is a layer of bismuth telluride. The bismuth telluride layer is illustrated in FIGS. 2D, 2E, 2F AND 2G of Pomerene et al. Significantly, Pomerene et al. describes the character of the bismuth telluride layer on col. 2, ll. 11-16. There, the patentees stated:

Peltier device 11 is typically fabricated from Peltier materials such as Bismuth Telluride (Bi_{1.5}sub.2 Te₃) or Lead Telluride (PbTe). In contrast to most metals that typically exhibit both high electrical and high thermal conductivity, Peltier materials exhibit very high electrical conductivity and relatively low thermal conductivity.

(Emphasis added).

Pomerene et al. clearly states that the Peltier effect device 11 is formed in the bismuth telluride conductor layer and thus not in an insulator substrate as set forth in Applicants' claims.

The foregoing applies generally to claims 1, 3-6, 9, 11-15 and 19. Applicants now address some of the rejected claims individually.

As to claims 3-7, Applicants respectfully submit that the additional limitations recited therein are not disclosed in Pomerene et al.

Claims 8-9 and 11 are patentable for the reasons advanced above with regard to claim 1.

Turning now to claim 12, Applicants submit that Pomerene et al. does not disclose a semiconductor island. In addition, claim 12 is patentable for the reasons advanced above with regard to claim 1.

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Claims 13-17 recite limitations in addition to those from base claims 12 that are not disclosed in Pomerene et al.

Claim 19 is patentable for the reasons advanced above with regard to claim 12.

Turning now to claim 20, Applicants submit that Pomerene et al. does not disclose a plurality of semiconductor islands.

As to claims 21-28, Pomerene et al. does not disclose the limitations from base claim 20 or from those dependent claims.

Rejections under 35 U.S.C. 103(a)

The Examiner rejected claims 7, 8, 16-18, 24, 25 and 27 under 35 U.S.C. 103(a) as being unpatentable over Pomerene et al. in view of Adler et al. As to claims 7, 8 and 16-18, Applicants submit that the combined teachings of Pomerene et al. and Adler et al. do not disclose a Peltier effect device positioned in an insulating substrate. This follows from the fact that the Pomerene et al. does not disclose a Peltier device positioned in an insulating substrate as set forth above in the discussion of claim 1.

Claim 20 distinguishes over the combined teachings of Pomerene et al. and Adler et al. because neither discloses a plurality of semiconductor island regions. Claim 24 is distinguishable for the reasons advanced above with regard to claim 20 in that there is no disclosure in Adler et al. or Pomerene et al. of a plurality of semiconductor islands. Finally, claim 27 is distinguishable over the teachings of Pomerene et al. and Adler et al. because neither of those references discloses a plurality of semiconductor islands.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 1, 3-9, 11-17 and 19-28 are patentable and respectfully request that a Notice of Allowability issue in due course.

Corrected Drawings

Applicants previously submitted two corrected drawing sheets, sheets 1 of 10 and 10 of 10, for the Examiner's approval.¹ Corrected sheet 1 of 10 changes present element number "30" to element number --36-- and includes element number --30-- for the active region beneath the circuit element 24. Corrected sheet 10 of 10 changes present element number "130" to element number --

¹The corrected drawing sheets were filed on March 28, 2003 concurrently with a Response to the Office Action Mailed December 10, 2002.

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136--, present element number "134" to element number --132--, and includes element number --130-- for the active region beneath the circuit element 124.

To date, the Examiner has not approved the corrected sheets. Applicants respectfully request approval of the two corrected sheets.

Interview Summary

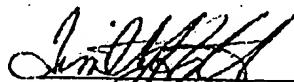
On September 25, 2003, the undersigned interviewed the Examiner by telephone regarding the substance of the instant Office Action. During the interview, claim 1 and the teachings of Pomerene et al. were discussed. The undersigned presented the argument set forth above regarding the teachings of Pomerene et al. as applied to claim 1. The Examiner advised that the matter would be taken under advisement and invited the submission of this paper.

Miscellaneous

The Assistant Commissioner is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:103HON.

Respectfully submitted,

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